

FIG. 1A  
(PRIOR ART)

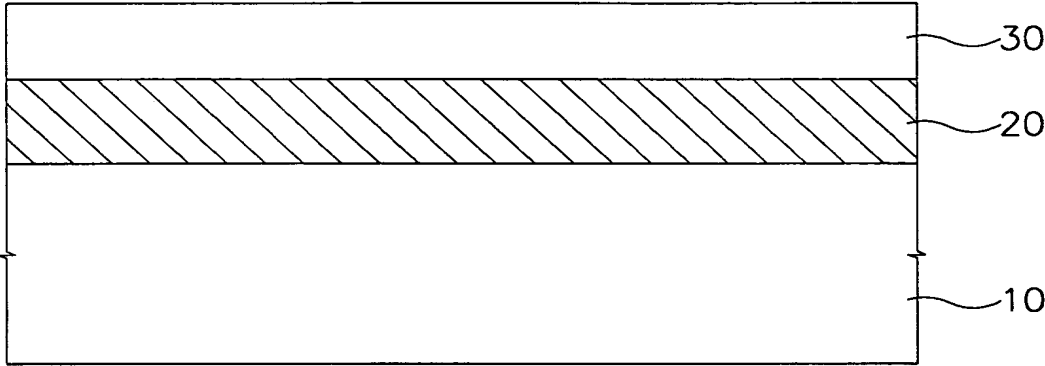


FIG. 1B  
(PRIOR ART)

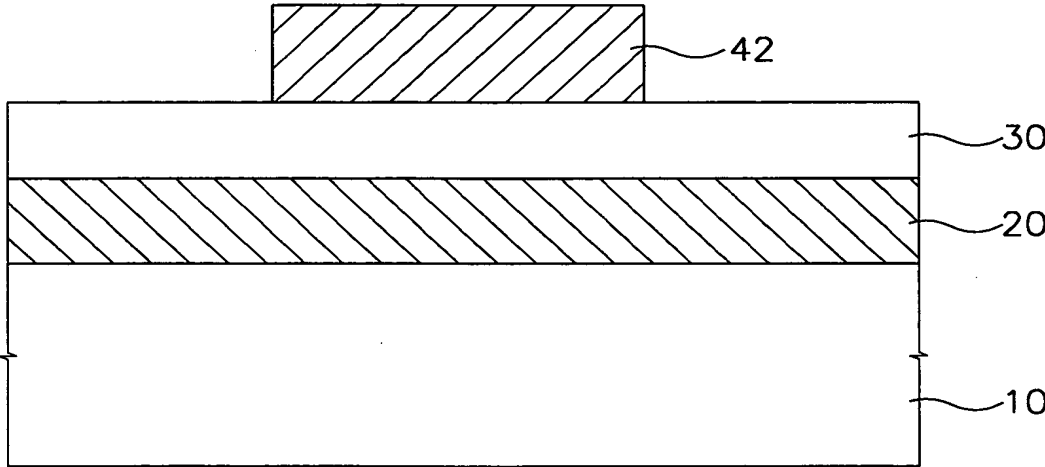


FIG. 1C  
(PRIOR ART)

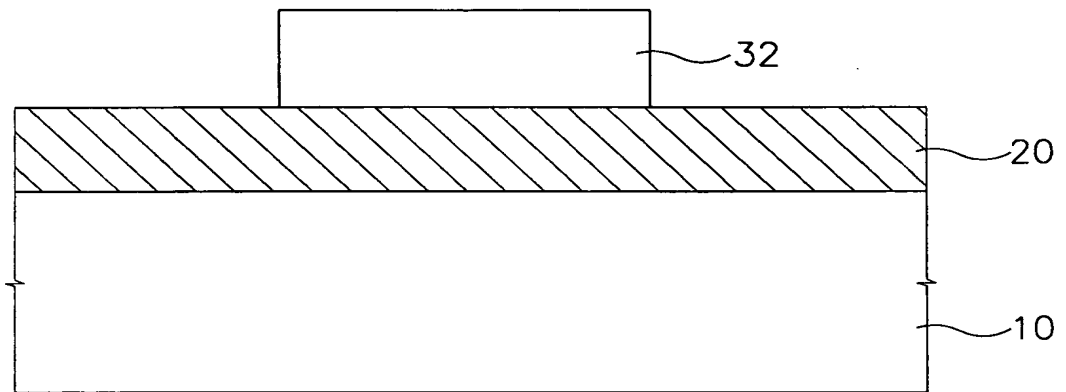
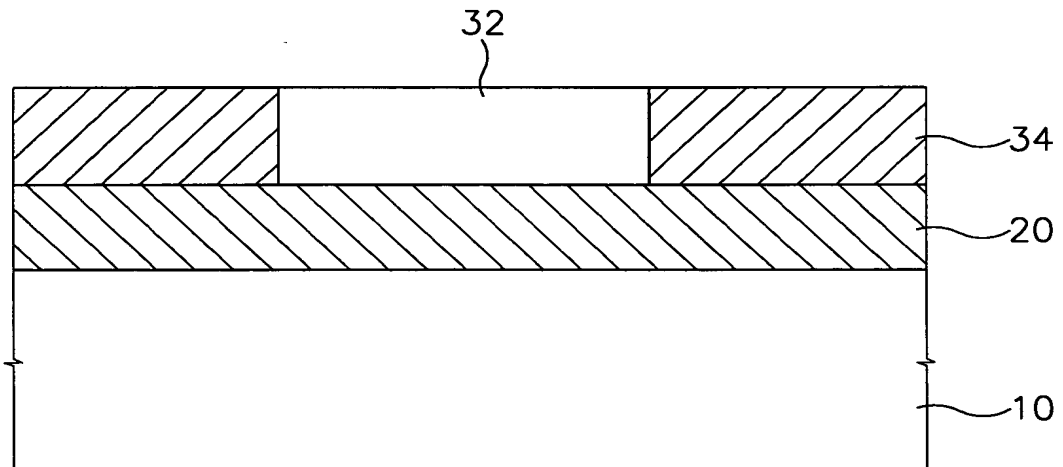


FIG. 1D  
(PRIOR ART)



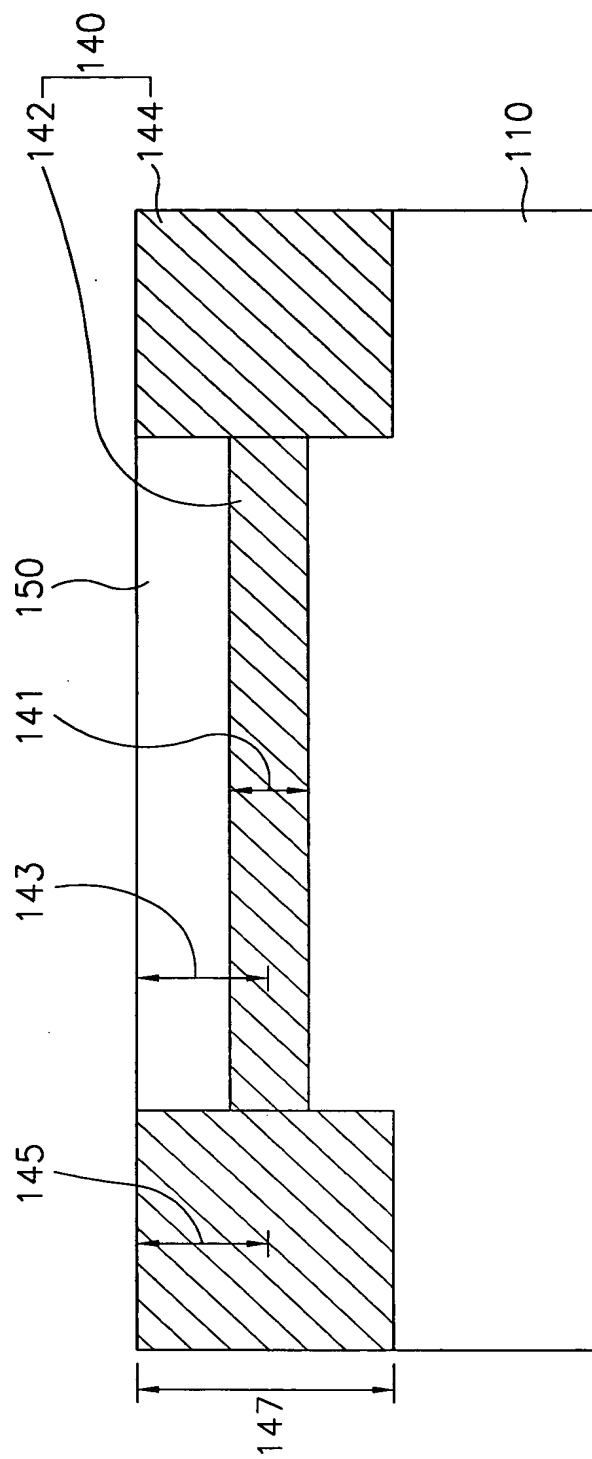
[illegible]

FIG. 3A

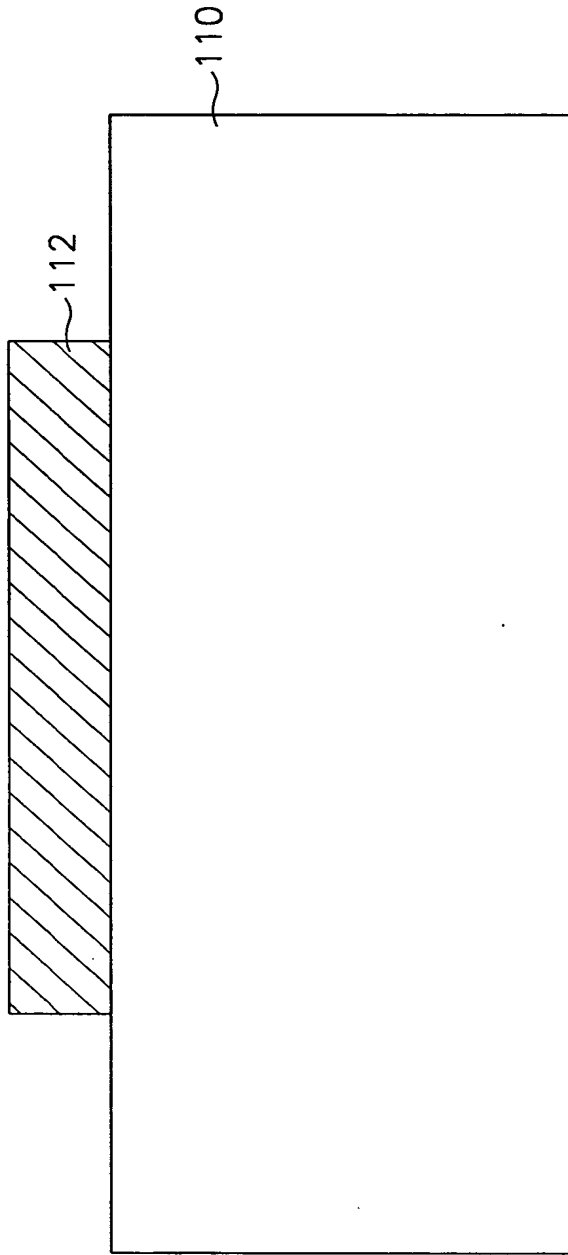


FIG. 3B

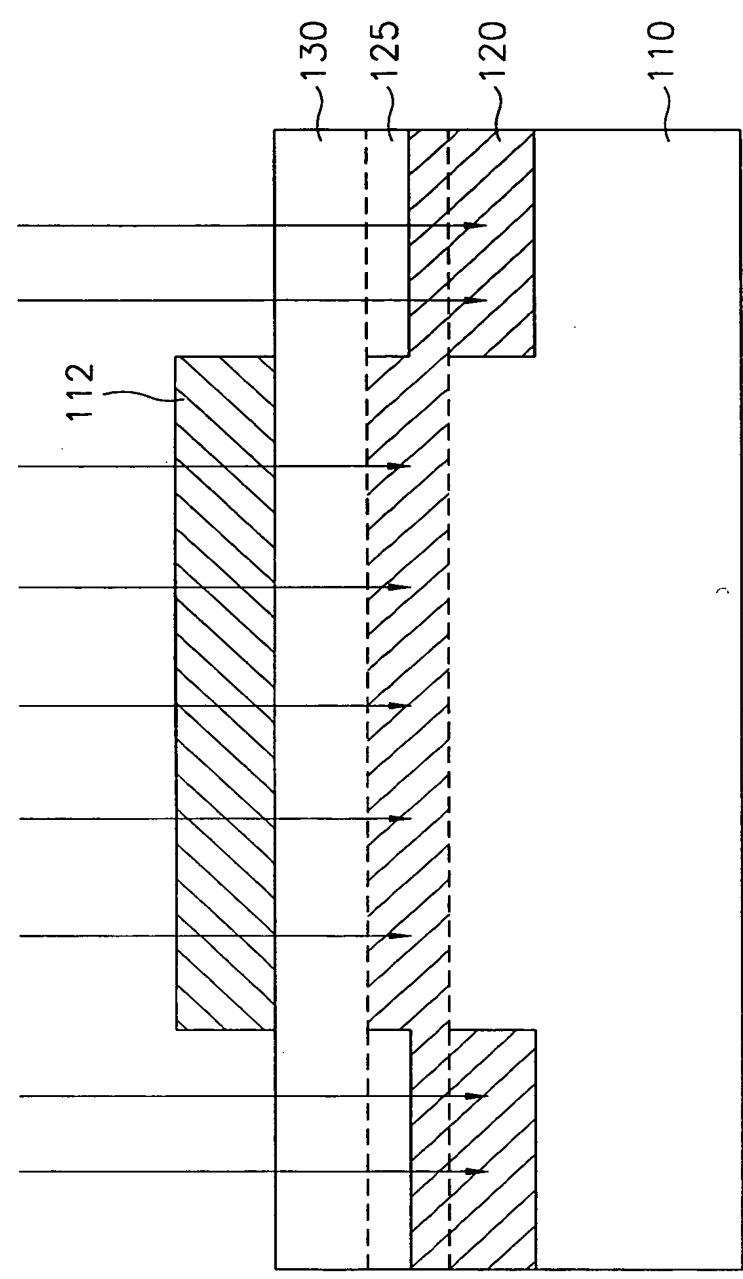
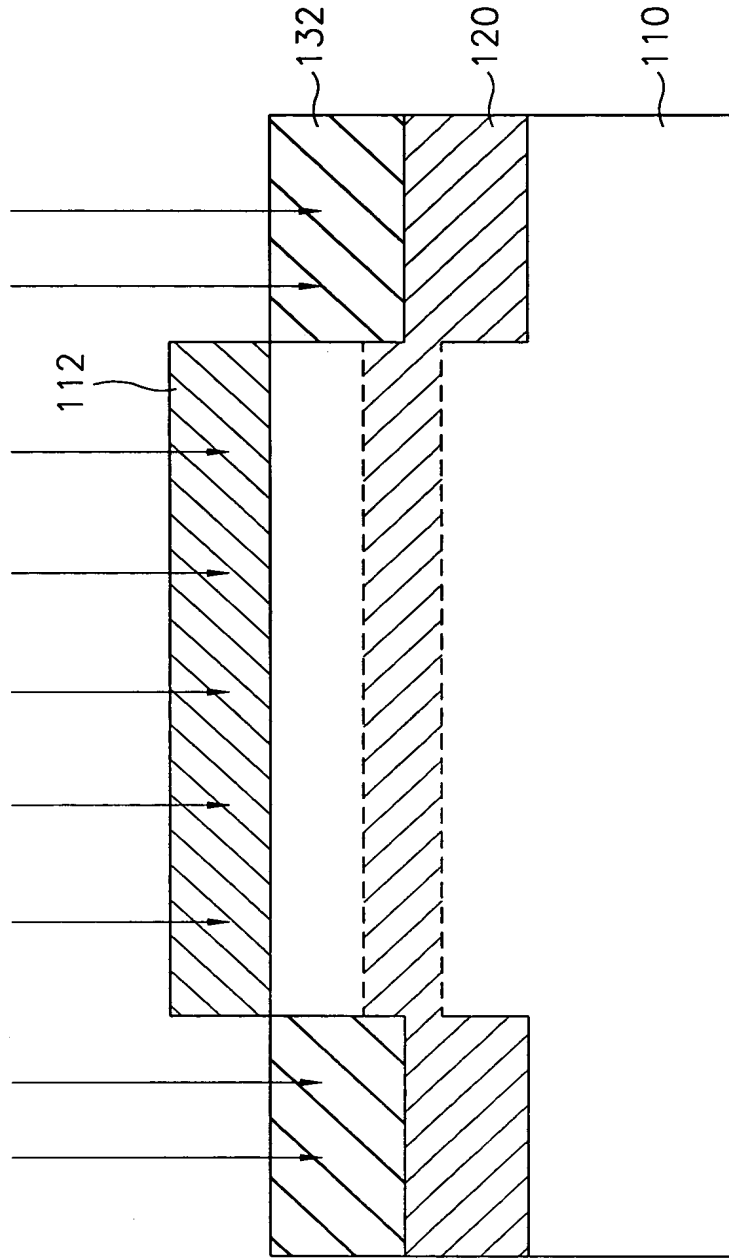


FIG. 3C



A cross-sectional view of a semiconductor device. A substrate 110 is shown at the bottom. A gate stack 140 is formed on the substrate, consisting of a gate dielectric layer and a gate electrode. A channel region 150 is formed in the substrate beneath the gate stack.

FIG. 4

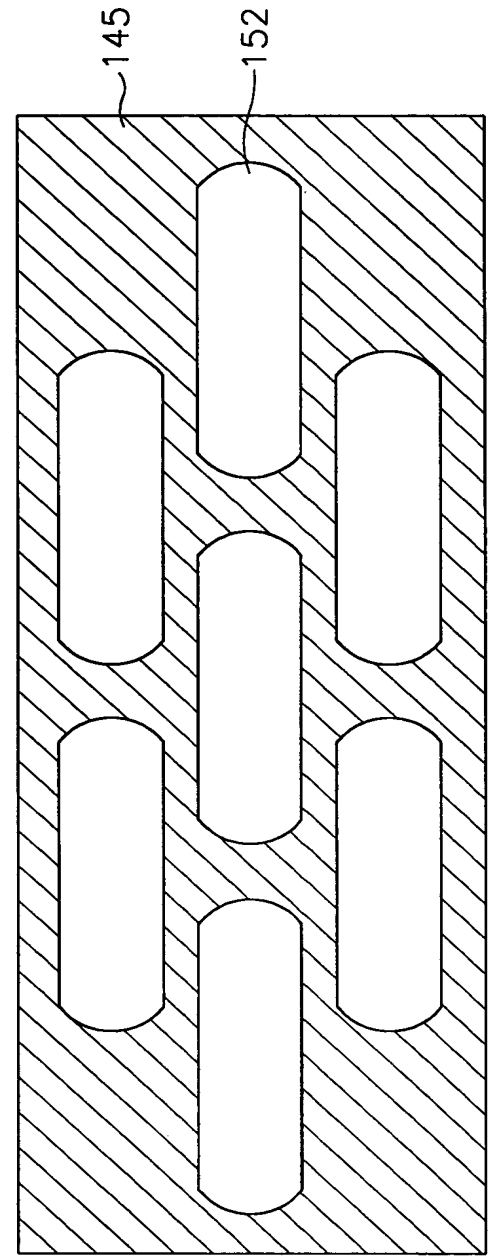




FIG. 5

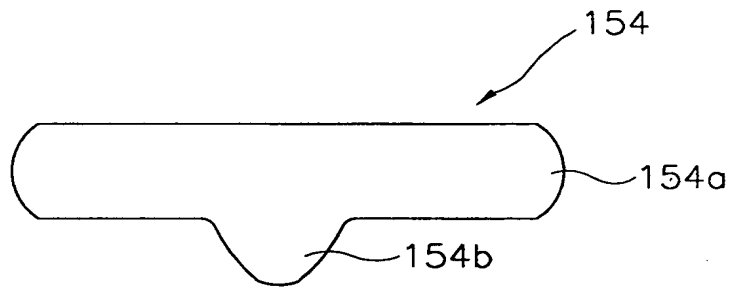


FIG. 6

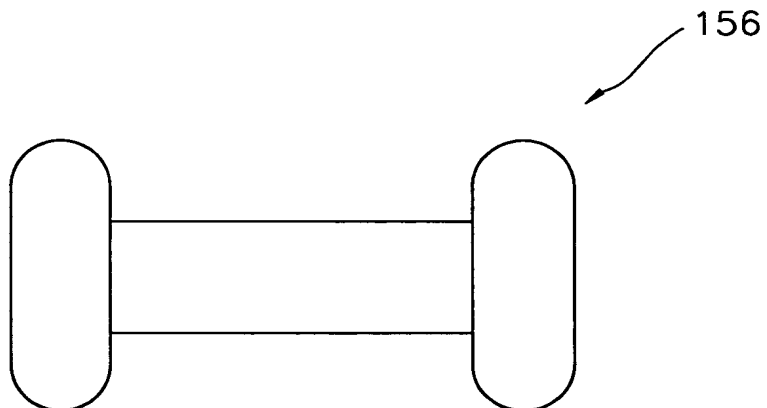


FIG. 7

